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| Texas A&M University |
| Lab 3: Cell Characterization |
| ECEN 454 |

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**Purpose:** This lab is intended to introduce students to cell characterization. Although there are many factors that can go into cell characterization, for this lab, the student will focus on delays and input capacitance. By modeling the NAND and XOR gates off of the circuits created in the previous lab, students will be able to see how these parameters effect circuits they’ve created.

**Procedure:**

1. Download all the necessary files from eCampus, and look over cell18.spi to understand what it is doing. Make a copy of demo.spi and rename it inverter.spi to use as the first simulation.
2. Run the simulation for inverter.spi. Open waveforms and import the waveform created from this simulation, located in the directory inverter.raw/, and click TransientAnalysis.
3. Click on tools > measurement and set a time domain to measure the delay from 50% to 50%. Drag the measurement box along the waveform to obtain rising delay and falling delay.
4. Modify inverter.spi with the values used in the previous lab for width of the nmos and pmos. Record the rising and falling delay, and compute the error between the two delays. If it is larger than 10%, change the widths of the nmos or pmos to get the error under 10%.
5. Copy the demo.spi file again and rename it inverter\_delaytable.spi. Remove the resistor, and change the output connection of the capacitor. Choose 15 values for the capacitor between 1fF and 100fF, and record the rising and falling delay for each value.
6. Use the file simcap.spi to run the AC simulation. Open the file and understand what it is doing. Run the simulation, and set up the measuring tool for a general Data(x,y) measurement. Add 10 of these measurements and use these to acquire sink capacitance.
7. Add NAND2 and XOR2 subckts to the cell18.spi file, and redo steps 1-6 for both of these gates.

**Results:**

1. The first inverter simulation was done without making any changes to the files, which resulted in a large difference between the rising and falling delay. After this, the inverter.spi file was modified to have a pmos width of 0.98um and a nmos width of 0.35um. The delays became closer in value, within a 10% error of one another, as shown below.

Text, email

Description automatically generated

Graphical user interface

Description automatically generated

1. The table below shows the rising and falling delay for different values of capacitance. As can be seen, the delays increase as the capacitance increases, but the error decreases as the capacitance increases.



1. For the AC simulation, the simulation file and waveform are displayed below with 10 sample points.

Graphical user interface

Description automatically generated

To calculate the sink capacitance for each point, the formula C = I/2\*pi\*f was used, and then the 10 results were averaged for an overall sink capacitance of 2.75fF.

1. After the inverter was completed, the NAND2 gate was connected on the cell18.spi, and simulation files for the NAND were made. The delay was observed for the default pmos and noms widths, and then was adjusted to have a pmos width of 0.65um and a nmos width of 0.3um to obtain rising and falling delay with a 0% error. The waveform and simulation file are displayed below.

Graphical user interface, text, email

Description automatically generated

A screenshot of a computer

Description automatically generated with medium confidence

1. The table below shows the rising and falling delay for different values of capacitance. As can be seen, the delays increase as the capacitance increases.



1. For the AC simulation, the waveform is displayed below with 10 sample points.

Graphical user interface, timeline

Description automatically generated

To calculate the sink capacitance for each point, the formula C = I/2\*pi\*f was used, and then the 10 results were averaged for an overall sink capacitance of 2.37fF.

1. After the inverter was completed, the XOR2 gate was connected on the cell18.spi, and simulation files for the XOR were made. The delay was observed for the default pmos and noms widths, and then was adjusted to have a pmos width of 1.2um and an nmos width of 0.2um to obtain rising and falling delay with a -0.2688% error. The simulation file and waveform are displayed below.

Graphical user interface, text, application, email

Description automatically generated

A screenshot of a computer

Description automatically generated with medium confidence

1. The table below shows the rising and falling delay for different values of capacitance. As can be seen, the delays increase as the capacitance increases, but the error decreases as the capacitance increases.



1. For the AC simulation, the waveform is displayed below with 10 sample points.

Diagram

Description automatically generated

To calculate the sink capacitance for each point, the formula C = I/2\*pi\*f was used, and then the 10 results were averaged for an overall sink capacitance of 5.02fF.

1. Finally, the cell18.spi file is included below with each subckt defined and connected. This file was made with reference to each circuit created in the previous lab.

Text

Description automatically generated

**Conclusion:** For the first task, it was learned that by decreasing/increasing the pmos width would increase/decrease the rising delay, while the same was true of the nmos width for the falling delay. For the second task, it was learned that generally, increasing output capacitance would increase the rising and falling delay, but decrease the error of the delays with respect to each other. Finally, for the last task, it was learned that the XOR gate had about twice as much sink capacitance as the NAND gate, suggesting a circuit with more transistors would result in a larger sink capacitance.